CLAIMS

1. An apparatus comprising:

a device comprising (i) a gate configured to receive an input voltage, (ii) a drain coupled to a first supply voltage, and (iii) a source coupled to an output; and

a resistive element coupled between said source and a second supply voltage, wherein said apparatus provides voltage tolerance between said input voltage and said output.

2. The apparatus according to claim 1, wherein said apparatus is further configured to provide fail-safe protection between said input voltage and said output.

3. The apparatus according to claim 1, wherein said device is configured in a source-follow configuration.

4. The apparatus according to claim 1, wherein said device comprises an NMOS device.

5. The apparatus according to claim 1, wherein said device comprises a native NMOS device.

6. The apparatus according to claim 1, wherein said apparatus is implemented in a low voltage differential circuit.

7. The apparatus according to claim 1, wherein said device comprises a PMOS device.

8. The apparatus according to claim 1, wherein said device comprises a native PMOS device.

9. The apparatus according to claim 1, wherein said first supply voltage comprises a ground voltage.

10. The apparatus according to claim 1, wherein said second supply voltage comprises a ground voltage.

11. A method for implementing voltage protection comprising the steps of:

configuring a device to have (i) a gate for receiving an input voltage, (ii) a drain for receiving a first supply voltage, and (iii) a source for presenting an output; and

configuring a resistive element between said source and a second supply voltage, wherein said device provides voltage tolerance between said input voltage and said output.

12. The method according to claim 11, wherein said method is further configured to provide fail-safe protection between said input voltage and said output.

13. The method according to claim 11, wherein said device is configured in a source-follow configuration.

14. The method according to claim 11, wherein said device comprises an NMOS device.

15. The method according to claim 11, wherein said device comprises a PMOS device.

16. The method according to claim 11, wherein said device comprises a native NMOS device.

17. The method according to claim 11, wherein said device comprises a native PMOS device.

18. An apparatus comprising:

a first stage comprising (A) a device comprising (i) a gate configured to receive an input voltage, (ii) a drain coupled to a first supply voltage, and (iii) a source coupled to a first output, and (B) a resistive element coupled between said source and a second supply voltage; and

a second stage comprising (A) a device comprising (i) a gate coupled to said first output, (ii) a drain coupled to said first supply voltage, and (iii) a source coupled to a second output, and (B) a resistive element coupled between said source and said first supply voltage, wherein said apparatus provides voltage tolerance between said input voltage and said output.

19. The apparatus according to claim 1, wherein said first and said second output are multiplexed to present a third output.

20. An apparatus comprising:

a first stage comprising (A) a device comprising (i) a gate configured to receive an input voltage, (ii) a drain coupled to a first supply voltage, and (iii) a source coupled to an output, and (B) a resistive element coupled between said source and a second supply voltage; and

a second stage comprising (A) a device comprising (i) a gate configured to receive said input voltage, (ii) a drain coupled to a first supply voltage, and (iii) a source coupled to said output, and (B) a resistive element coupled between said source and a second supply voltage, wherein said apparatus provides voltage tolerance between said input voltage on said output.